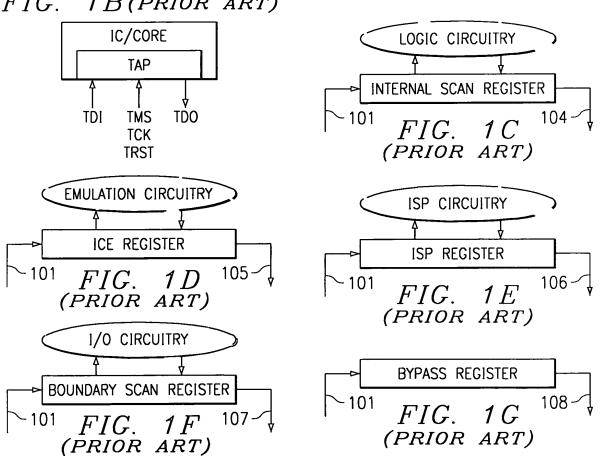


FIG. 1B(PRIOR ART)



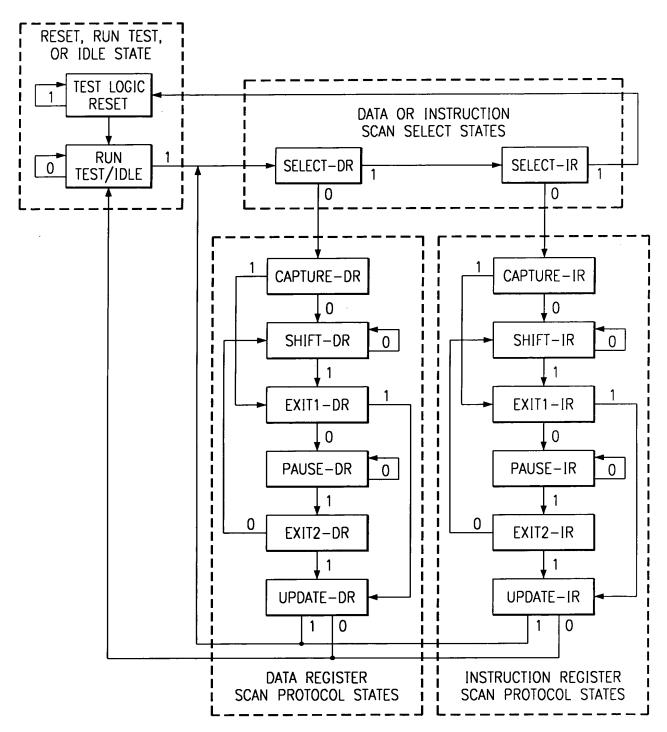


FIG. 2 (PRIOR ART)

FIG. 3A
(PRIOR ART)

LOGIC CIRCUITRY

SE INTERNAL SCAN REGISTER SO

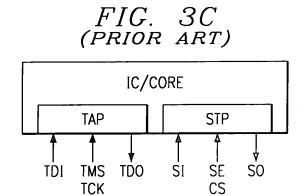
SE CS CK

FIG. 3B
(PRIOR ART)

IC/CORE

STP

SI SE SO
CS
CK



CK

TRST

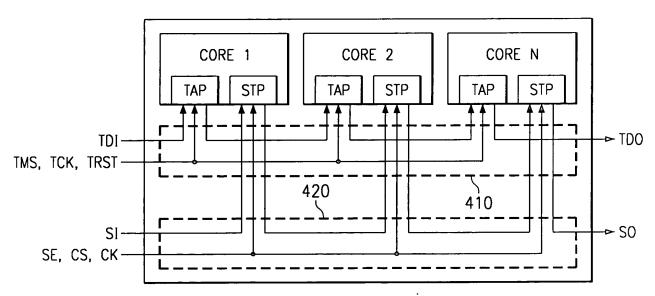


FIG. 4 (PRIOR ART)